探境科技
INTENGINE

# Voitist 611 (VOI611)

## Embedded Deep Learning
## Speech Recognition Chip

# Data Sheet

(V 1.50)

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# Table of Contents

# 1. General Introduction

Voitist 611 (abbreviate as VOI611) is an automatic speech recognition (ASR) chip for embedded products based on local deep learning inference. It integrates one self-developed neural processing unit (NPU), one ARM Cortex-M3 processor, on-chip memory, and various peripheral interfaces.

VOI611 can efficiently accelerate various neural networks inference to quickly recognize many voice key words offline both in near field and far field, even in a noisy environment.

With VOI611, users can easily control target equipment without the Internet connection by issuing simple voice commands.

This IC can be applicate to Smart Home, Smart Vehicle, Intelligent Sound Box and Man-machine interactive product. It has excellent performance, high flexibility and low power consumption.

# 2. Chip Architecture

VOI611 is an automatic speech recognition (ASR) chip for embedded products based on local deep learning inference. The highlights of the chip include following features:

- Self-developed neural process unit (NPU) that enables chipset to run deep learning model locally
- Powerful ARM 32bit Cortex-M3 processor
- QSPI interface for external Flash connection
- Audio interfaces:

  I2S, PDM input, analog microphone input, analog audio output
- Peripheral interfaces:

  PWM output, I2C, UART, SPI, GPIO
- JTAG debug interface
- On-chip PLL, timer and watch dog

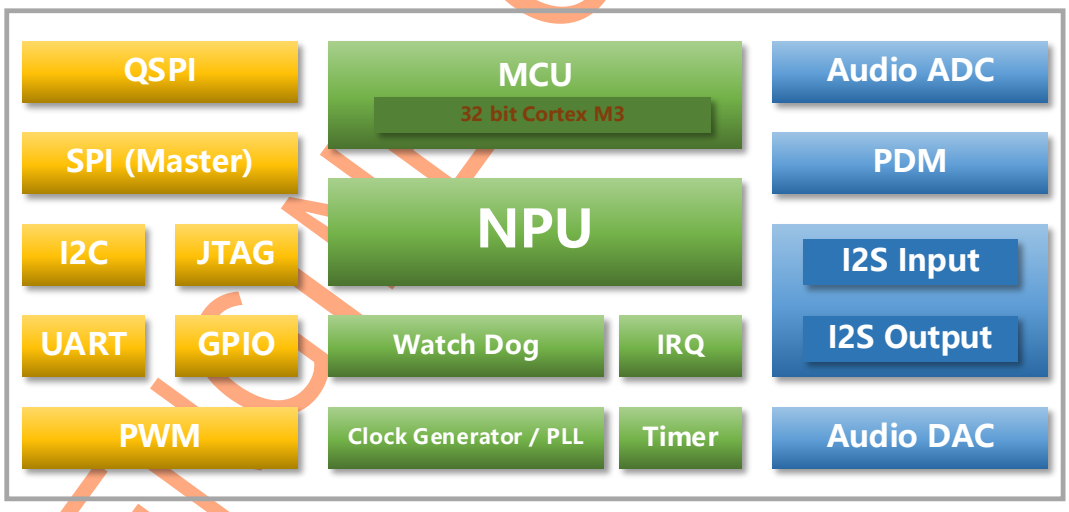



**Figure 2-1 VOI611 Chip Block Diagram**

# 3. Feature List

## 3.1. ASR Performance

- Interactive Steps:

  Wake up Word Input → Response → Command Speech Input → Recognition → Feedback (TTS output and circuit action)
- Key words support: up to 200 voice key words, 3~6 syllable for each key word
- Feedback speed: < 0.1s (time from speech input done to output feedback)
- Recognition ratio: > 98% under 60dB environment noise
- Speech Q&A support: up to 5 layer
- Support Languages: mandarin Chinese and English
- Operating Range: >5m
- Speech Input: Support analog and digital microphone, support far field recognition, noise suppression and sound source localization
- Feedback mode: TTS output and execution circuit control
- TTS output: TTS content customizable
- Development support:
  - Support customer secondary development
  - Providing customized development services

## 3.2. MCU

- Powerful ARM 32bit Cortex-M3 processor
- Clock speed up to 131 MHz
- 512KB on chip memory

## 3.3. NPU

- The NPU base Intengine Technology owned Storage First Architecture (SFA) include following features:
  - Support all popular speech neural network topologies
  - High efficiency of local reasoning

## 3.4. Firmware Storage

- External QSPI Flash is used as the firmware storage
- Min. flash memory size request 4MB

## 3.5. Peripheral Interface

- I2S digital audio I/F: 1 port input & 1 port output, Master or Slave mode,
- PDM digital audio input interface: 1 port ( L / R )
- Analog Mic input: 1 port ( L / R )
- Analog audio output: 1 port ( L / R )
- PWM output: 4 ports
- I2C I/F: 1 port, Master mode
- UART I/F: 2 ports, support max. Bps to 115200
- SPI I/F: 1 port, Master mode，with 65.5MHz clock
- QSPI I/F: 1 port, for SPI Flash connection
- GPIO: 16 pins, multiplexed with other pins

## 3.6. Debug Interface

- **Both JTAG and UART are supported for software debug**

## 3.7. Timer Resource

- Timer: 3
- Watch Dog Timer: 1

## 3.8. Audio ADC Characteristics

- High Resolution Stereo Sigma-Delta audio ADC
- ADC inside PGA with Max. gain 27dB
- Full-Amplitude Input Voltage: 2.1Vp-p

## 3.9. Clock & Power

- Clock:
  - On-chip PLL
  - On-chip oscillator with external 24.576 MHz crystal
- Power Voltage:
  - Operating Voltages: 3.3V
  - Core Voltages: 1.2V
- Power Consumption:
  - Sleep mode: <15mW
  - Recognition mode: 100~150mW

# 4. Pin Map

## 4.1. Pin Map Figure

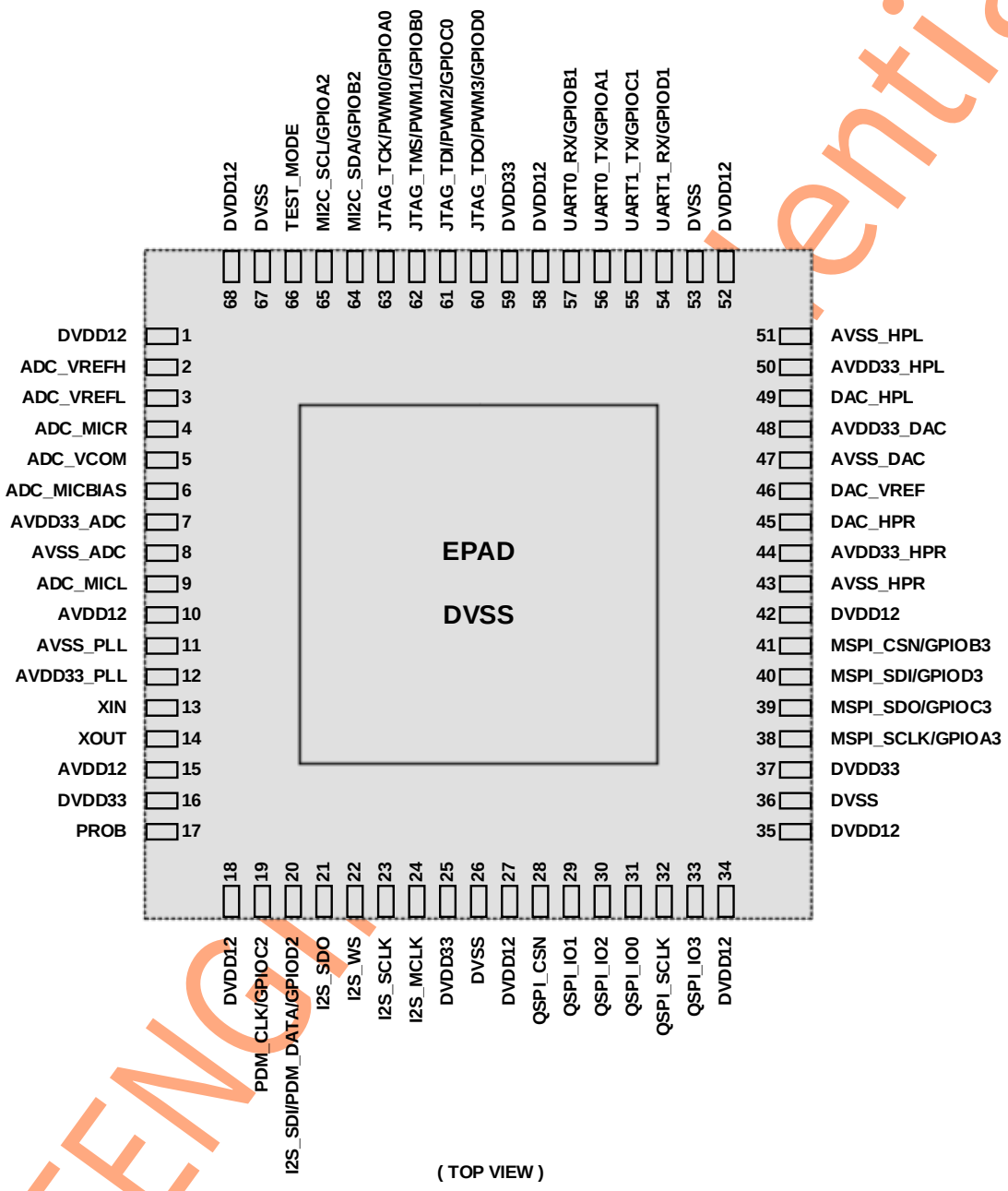



**Figure 4-1 Pin Map Figure**

## 4.2. Power and Ground Pins

| Pin Number | Signal | Type | Description |
|---|---|---|---|
| 1,18,27,34,35, 42,52,58,68 | DVDD12 | DP | 1.2V digital power for core |
| 10,15 | AVDD12 | AP | 1.2V analog power for PLL |
| 16,25,37,59 | DVDD33 | DP | 3.3V digital power for IO |
| 12 | AVDD33_PLL | AP | 3.3V analog power for PLL |
| 7 | AVDD33_ADC | AP | 3.3V analog power for ADC |
| 2 | ADC_VREFH | AI | ADC reference voltage; A 10uF in parallel with a 0.1uF ceramic capacitor attached from this pin to AVSS_ADC |
| 3 | ADC_VREFL | AI | ADC reference voltage; A 10uF in parallel with a 0.1uF ceramic capacitor attached from this pin to AVSS_ADC |
| 5 | ADC_VCOM | AO | Common voltage reference output; A 4.7uF in parallel with a 0.1uF ceramic capacitor attached from this pin to AVSS_ADC; The output voltage is 1.65V |
| 6 | ADC_MIBIAS | AO | Electrets Microphone Bias, the output voltage is 1.6~2.8V, output load capacitor no less than 4.7uF |
| 48 | AVDD33_DAC | AP | 3.3V analog power for DAC |
| 46 | DAC_VREF | AO | DAC internal reference voltage; A 10uF in parallel with a 0.1uF ceramic capacitor attached from this pin to AVSS_DAC |
| 50 | AVDD33_HPL | AP | 3.3V analog power for left channel of speaker |
| 44 | AVDD33_HPR | AP | 3.3V analog power for right channel of speaker |
| 26,36,53,67, EPAD | DVSS | DG | Digital ground |
| 11 | AVSS_PLL | AG | Analog ground for PLL |
| 8 | AVSS_ADC | AG | Analog ground for ADC |
| 47 | AVSS_DAC | AG | Analog ground for DAC |
| 51 | AVSS_HPL | AG | Analog ground for left channel of speaker |
| 43 | AVSS_HPR | AG | Analog ground for right channel of speaker |

## 4.3. Audio Interface Signals

| Pin Number | Signal | Type | Description |
|---|---|---|---|
| 4 | ADC_MICR | AI | ADC input<br>(right channel of microphone) |
| 9 | ADC_MICL | AI | ADC input<br>(left channel of microphone) |
| 19 | PDM_CLK | I | PDM clock; Pull-down inside chip |
| | GPIOC2 | IO | GPIOC2; Pull-down inside chip |
| 20 | I2S_SDI | I | I2S data input; Pull-down inside chip |
| | PDM_DATA | I | PDM data input; Pull-down inside chip |
| | GPIOD2 | IO | GPIOD2; Pull-down inside chip |
| 21 | I2S_SDO | O | I2S data output; Pull-down inside chip |
| 22 | I2S_WS | O | I2S channel select;<br>Pull-down inside chip |
| 23 | I2S_SCLK | O | I2S serial clock; Pull-down inside chip |
| 24 | I2S_MCLK | O | I2S system clock;<br>Pull-down inside chip |
| 45 | DAC_HPR | AO | DAC data output<br>(right channel of speaker) |
| 49 | DAC_HPL | AO | DAC data output<br>(left channel of speaker) |

## 4.4. Control Interface Signals

| Pin Number | Signal | Type | Description |
|---|---|---|---|
| 28 | QSPI_CSN | O | QSPI mode select;<br>Pull-up inside chip |
| 29 | QSPI_IO1 | IO | QSPI data1; Pull-down inside chip |
| 30 | QSPI_IO2 | IO | QSPI data2; Pull-down inside chip |
| 31 | QSPI_IO0 | IO | QSPI data0; Pull-down inside chip |
| 32 | QSPI_SCLK | O | QSPI clock; Pull-down inside chip |
| 33 | QSPI_IO3 | IO | QSPI data3; Pull-down inside chip |
| 38 | MSPI_SCLK | O | Master SPI clock;<br>Pull-down inside chip |
| | GPIOA3 | IO | GPIOA3; Pull-down inside chip |
| 39 | MSPI_SDO | O | Master SPI data output;<br>Pull-down inside chip |
| | GPIOC3 | IO | GPIOC3; Pull-down inside chip |
| 40 | MSPI_SDI | I | Master SPI data input;<br>Pull-down inside chip |
| | GPIOD3 | IO | GPIOD3; Pull-down inside chip |
| 41 | MSPI_CSN | O | Master SPI mode select;<br>Pull-up inside chip |
| | GPIOB3 | IO | GPIOB3; Pull-up inside chip |
| 54 | UART1_RX | I | UART1 input; Pull-up inside chip |
| | GPIOD1 | IO | GPIOD1; Pull-up inside chip |
| 55 | UART1_TX | O | UART1 output; Pull-up inside chip |
| | GPIOC1 | IO | GPIOC1; Pull-up inside chip |
| 56 | UART0_TX | O | UART0 output; Pull-up inside chip |
| | GPIOA1 | IO | GPIOA1; Pull-up inside chip |
| 57 | UART0_RX | I | UART0 input; Pull-up inside chip |
| | GPIOB1 | IO | GPIOB1; Pull-up inside chip |
| 64 | MI2C_SDA | IO | I2C data; Pull-up inside chip |
| | GPIOB2 | IO | GPIOB2; Pull-up inside chip |
| 65 | MI2C_SCL | O | I2C clock; Pull-up inside chip |
| | GPIOA2 | IO | GPIOA2; Pull-up inside chip |

## 4.5. System Function Signals

| Pin Number | Signal | Type | Description |
|---|---|---|---|
| 13 | XIN | I | Input for crystal connection |
| 14 | XOUT | O | Output for crystal connection |
| 17 | PROB | I | System reset (Active low);<br>Pull-up inside chip |
| 60 | JTAG_TDO | O | JTAG data output;<br>Pull-down inside chip |
| | PWM3 | AO | PWM3 output; Pull-down inside chip |
| | GPIOD0 | IO | GPIOD0; Pull-down inside chip |
| 61 | JTAG_TDI | I | JTAG data input;<br>Pull-down inside chip |
| | PWM2 | AO | PWM2 output; Pull-down inside chip |
| | GPIOC0 | IO | GPIOC0; Pull-down inside chip |
| 62 | JTAG_TMS | I | JTAG mode select;<br>Pull-down inside chip |
| | PWM1 | AO | PWM1 output; Pull-down inside chip |
| | GPIOB0 | IO | GPIOB0; Pull-down inside chip |
| 63 | JTAG_TCK | I | JTAG clock; Pull-down inside chip |
| | PWM0 | AO | PWM0 output; Pull-down inside chip |
| | GPIOA0 | IO | GPIOA0; Pull-down inside chip |
| 66 | TEST_MODE | I | Test usage (usually connect GND);<br>Pull-down inside chip |

# 5. Typical Application

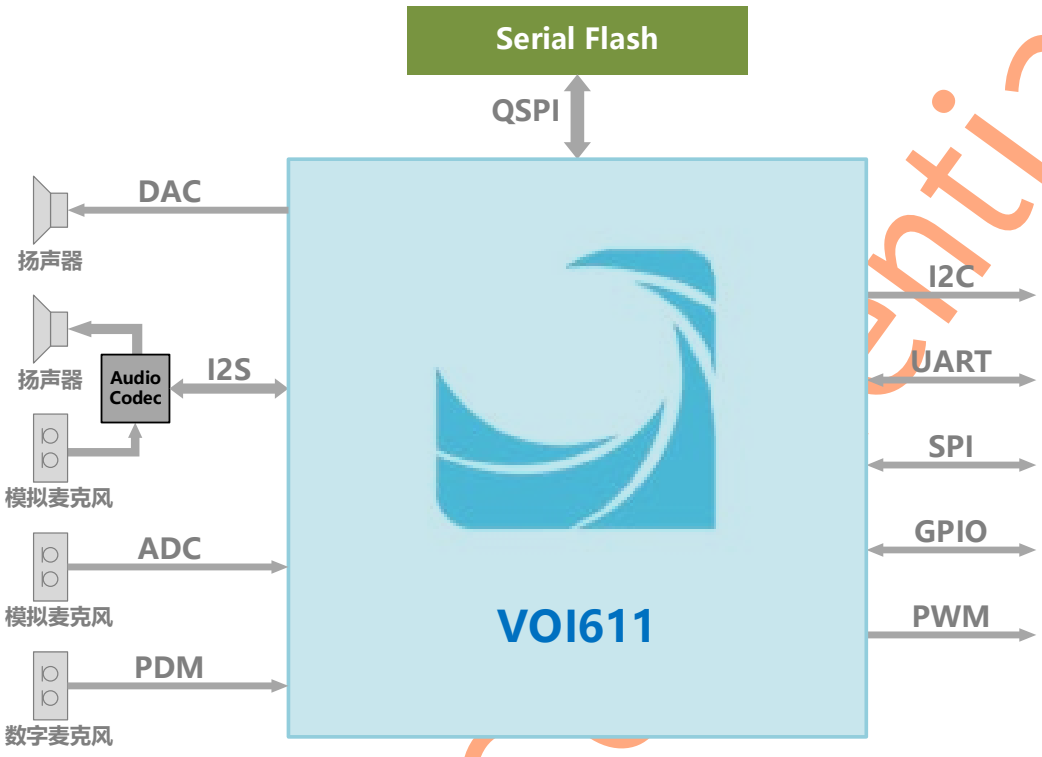



**Figure 5-1 5. Typical Application Diagram**

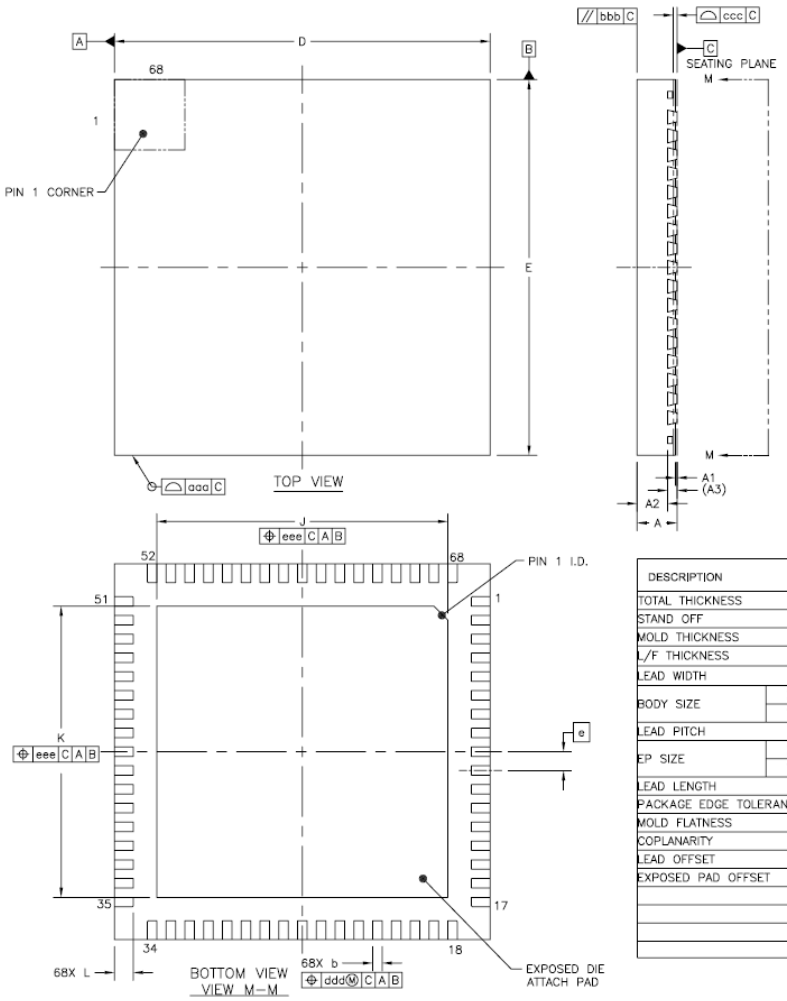
# 6. Electronic Specification

The electronic specification with recommended operating conditions as below table:

| Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Core Power Supply Voltage | DVDD12 | 1.14 | 1.2 | 1.26 | V |
| Core Power Supply Current | | | 80 | | mA |
| 1.2V Analog Power Supply Voltage | AVDD12 | 1.14 | 1.2 | 1.26 | V |
| Digital I/O Power Supply Voltage | DVDD33 | 3.0 | 3.3 | 3.6 | V |
| 3.3V PLL Power Supply Voltage | AVDD33_PLL | 3.14 | 3.3 | 3.46 | V |
| 3.3V ADC Power Supply Voltage | AVDD33_ADC | 3.14 | 3.3 | 3.46 | V |
| 3.3V DAC Power Supply Voltage | AVDD33_DAC | 3.14 | 3.3 | 3.46 | V |
| 3.3V HPL Power Supply Voltage | AVDD33_HPL | 3.14 | 3.3 | 3.46 | V |
| 3.3V HPR Power Supply Voltage | AVDD33_HPR | 3.14 | 3.3 | 3.46 | V |
| SPI Clock frequency | SPI Clock | 0.002 | | 65.536 | MHz |
| Operating Ambient Temperature | Tamb | -25 | | 85 | ℃ |
| Storage Temperature | Tstg | -55 | | 125 | ℃ |
| Moisture Sensitivity Level | MSL | | 3 | | Level |
| Electro-Static Discharge | ESD | | 2000 | | V |

# 7. Package Information

Package Specification (Unit: mm): QFN68-8x8x0.85 RoHS package




| DESCRIPTION | | SYMBOL | MILLIMETER | | |
|---|---|---|---|---|---|
| | | | MIN | NOM | MAX |
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.035 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | 0.67 |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.15 | 0.20 | 0.25 |
| BODY SIZE | X | D | 8 BSC | | |
| | Y | E | 8 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| EP SIZE | X | J | 6.1 | 6.2 | 6.3 |
| | Y | K | 6.1 | 6.2 | 6.3 |
| LEAD LENGTH | | L | 0.35 | 0.4 | 0.45 |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.1 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

**Figure 7-1 QFN68 Package Specification**